

**APPLICATION
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TITLE: LATERAL PHASE CHANGE MEMORY

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LATERAL PHASE CHANGE MEMORY

Background

This invention relates generally to phase change memories.

Phase change memories use phase change materials, 5 i.e., materials that may be electrically switched between a generally amorphous and a generally crystalline state, as an electronic memory. One type of memory element utilizes a phase change material that may be, in one application, electrically switched between generally amorphous and 10 generally crystalline local orders or between detectable states of local order across the entire spectrum between completely amorphous and completely crystalline states.

Typical materials suitable for such an application include various chalcogenide elements. The state of the 15 phase change materials is also non-volatile. When the memory is set in either a crystalline, semi-crystalline, amorphous, or semi-amorphous state representing a resistance value, that value is retained until reprogrammed, even if power is removed. This is because 20 the program value represents a phase or physical state of the material (e.g., crystalline or amorphous).

Thus, there is a need for different ways to make phase change memories.

Brief Description of the Drawings

Figure 1 is a greatly enlarged cross-sectional view of one embodiment of the present invention;

5 Figure 2 is a greatly enlarged cross-sectional view at an early stage of manufacture in accordance with one embodiment of the present invention;

Figure 3 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

10 Figure 4 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 5 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one 15 embodiment of the present invention;

Figure 6 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

20 Figure 7 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 8 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 9 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

5 Figure 10 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

Figure 11 is a greatly enlarged cross-sectional view at a subsequent stage of manufacture in accordance with one embodiment of the present invention; and

10 Figure 12 is a system schematic depiction of one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a pair of side-by-side cells 10 are formed over a substrate 26, in one embodiment of the 15 present invention. Each cell 10 includes a phase change material 36 between a pair of laterally displaced resistive electrodes 34 on either side of the phase change material 36.

For example, a top electrode 40 may be coupled to a 20 column line and an electrode 34 may be coupled to a row conductive line 44. Of course, the designations "row" and "column" may be reversed and are merely used for convenience.

In one embodiment, the cells 10 may be on the same 25 conductive line 44, each cell 10 selectively coupled to the line 44 by a selection device 42. The selection devices 42

may be, for example, field effect transistors, diodes, or a chalcogenide alloy rich in Selenium as three examples. The selection devices 42 and the conductive line 44 may be formed in a substrate 26 in one embodiment of the present

5 invention.

The selection device 42 may be coupled to a bottom electrode 24. The bottom electrodes 24 of the cells 10 may be separated by an insulator 30. On opposed sides of the insulator 30 is a liner 20. The liner 20 electrically

10 couples the bottom electrode 24 to a resistive electrode 34 associated with each cell 10.

Outbound of each electrode 34 is a phase change material 36 that may extend vertically and may be described as L-shaped in one embodiment. Outbound of the phase

15 change material 36 is an opposed electrode 34. Thus, the phase change cells 10 are arranged laterally so that the electrodes 34 are spaced apart in a horizontal direction, sandwiching intermediate phase change material 36.

The cells 10 may be formed within a dielectric layer

20 22 and another dielectric layer 30. A light transmissive material 38 such as a dielectric glass or a high bandgap and electrically insulating material 38, such as arsenic sulfide (As_2S_3), may also be positioned between the respective cells 10. In some embodiments of the present

25 invention, each cell 10 may be electrically addressed for programming, reading, or writing. In one embodiment, the

cells 10 may be optically addressed, two at a time, by a light signal, as indicated, to provide an extra dimension of cell 10 access.

Referring to Figure 2, a pair of spaced bottom 5 electrodes 24 may be defined over a substrate 26. The bottom electrodes 24 may be formed of aluminum as one example. The bottom electrodes 24 may be shaped or isolated.

A layer 22 of dielectric material may be formed over 10 the substrate 26 on the bottom electrode 24, followed by an etch stop layer 25, followed by an additional layer 22a. A first trench 46 may be formed centrally therethrough. In one embodiment, the layers 22, 22a may be oxide.

As shown in Figure 3, the conductive liner 20 may be 15 deposited into the first trench 46 and over the layer 22a. In one embodiment, the liner 20 may be tungsten or another strong conductor. As shown in Figure 4, the portion of the liner 20 at the bottom of the first trench 46, as well as a portion overlying the layer 22a, may be cleared down to the 20 etch stop layer 25, for example, using directional etching techniques.

Turning next to Figure 5, the structure of Figure 4 may be covered by an insulator 30 that may be deposited into the first trench 46 and over the insulator 22. The 25 insulator 30 may be, for example, silicon nitride. The

insulator 30 may act as a subsequent chemical mechanical polishing stop in some embodiments.

Next, as shown in Figure 6, a second trench 38 may be formed using an etchant that does not attack the liner 20 5 using a mask 32. Then, as shown in Figure 7, a resistive electrode 34 may be deposited, for example, using chemical vapor deposition. In one embodiment, the resistive electrode 34 may include titanium silicon nitride. As shown in Figure 8, the resistive electrode 34 may be 10 cleared at the bottom of the second trench 38 and atop of the island 39 and over the mask 32.

Thereafter, the phase change material 36 may be deposited by a chemical vapor deposition process so that a uniform conformal growth occurs on the side of electrode 15 34. An *in situ* backsputter may be utilized to remove a central region of that material 36 so that electrical contact between the two cells is broken. An L-shaped phase change material 36 results. Then the remaining structure may be filled with a chalcogenide light transmissive 20 material 38, such as As_2S_3 , in one embodiment of the present invention. As shown in Figure 11, this process may be followed by a chemical mechanical polishing that stops on the layer 30. Thereafter, as shown in Figure 1, the electrodes 40 may be patterned and deposited.

25 In one embodiment, the phase change material 36 may be a non-volatile, phase change material. A phase change

material may be a material having electrical properties (e.g., resistance) that may be changed through the application of energy such as, for example, heat, light, voltage potential, or electrical current.

5 Examples of phase change materials may include a chalcogenide material or an ovonic material. An ovonic material may be a material that undergoes electronic or structural changes and acts as a semiconductor once subjected to application of a voltage potential, electrical
10 current, light, heat, etc. A chalcogenide material may be a material that includes at least one element from column VI of the periodic table or may be a material that includes one or more of the chalcogen elements, e.g., any of the elements of tellurium, sulfur, or selenium. Ovonic and
15 chalcogenide materials may be non-volatile memory materials that may be used to store information.

In one embodiment, the phase change material 36 may be chalcogenide element composition from the class of tellurium-germanium-antimony ($Te_xGe_ySb_z$) material or a
20 GeSbTe alloy, although the scope of the present invention is not limited to just these materials.

The phase change material 36 may be programmed into one of at least two memory states by applying an electrical signal to the material 36. An electrical signal may alter
25 the phase of the material 36 between a substantially crystalline state and a substantially amorphous state,

wherein the electrical resistance of the material 36 in the substantially amorphous state is greater than the resistance of the material 36 in the substantially crystalline state. Accordingly, in this embodiment, the 5 material 36 may be adapted to be altered to one of at least two resistance values within a range of resistance values to provide single bit or multi-bit storage of information.

Programming of the material 36 to alter the state or phase of the material may be accomplished by applying 10 voltage potentials to the lines 40 and 44, thereby generating a voltage potential across the material 36. An electrical current may flow through a portion of the material 36 in response to the applied voltage potentials, and may result in heating of the material 36.

15 This heating and subsequent cooling may alter the memory state or phase of the material 36. Altering the phase or state of the material 36 may alter an electrical characteristic of the material 36. For example, the resistance of the material 36 may be altered by altering 20 the phase of the material 36. The material 36 may also be referred to as a programmable resistive material or simply a programmable material.

In one embodiment, a voltage potential difference of about 3 volts may be applied across a portion of the 25 material 36 by applying about 3 volts to a lower line 44 and about zero volts to an upper line 40. A current

flowing through the material 36 in response to the applied voltage potentials may result in heating of the material. This heating and subsequent cooling may alter the memory state or phase of the material.

5 In a "reset" state, the material 36 may be in an amorphous or semi-amorphous state and in a "set" state, the material may be in a crystalline or semi-crystalline state. The resistance of the material in the amorphous or semi-amorphous state may be greater than the resistance of the 10 material in the crystalline or semi-crystalline state. The association of reset and set with amorphous and crystalline states, respectively, is a convention. Other conventions may be adopted.

15 Due to electrical current, the material 36 may be heated to a relatively higher temperature to amorphisize memory material and "reset" memory material (e.g., program memory material to a logic "0" value). Heating the volume of material to a relatively lower crystallization temperature may crystallize memory material and "set" 20 memory material (e.g., program memory material to a logic "1" value). Various resistances of material 36 may be achieved to store information by varying the amount of current flow and duration through the volume of material.

25 The information stored in material 36 may be read by measuring the resistance of the material 36. As an example, a read current may be provided to the material 36

using opposed lines 40, 44 and a resulting read voltage across the memory material may be compared against a reference voltage using, for example, a sense amplifier (not shown). The read voltage may be proportional to the 5 resistance exhibited by the memory storage element. Thus, a higher voltage may indicate that material is in a relatively higher resistance state, e.g., a "reset" state. A lower voltage may indicate that the material is in a relatively lower resistance state, e.g., a "set" state. A 10 current based system may also be used.

In some embodiments of the present invention, a lateral plate design may have symmetry in all directions leading to an approximately rectangular chalcogenide volume. Thus, such a design may give uniformity to the 15 electric field, current flow, power dissipation and heat flow in some embodiments. Because of the design, the total volume of phase change material 36 may change phase, promoting tight resistance states from one programming event to another, reducing erratic programming, loss of 20 dynamic range, resistance or endurance issues, or possible alloy changes phase during programming event in some embodiments.

Turning to Figure 5, a portion of a system 500, in accordance with an embodiment of the present invention, may 25 be used in wireless devices such as, for example, a personal digital assistant (PDA), a laptop or portable

computer with wireless capability, a web tablet, a wireless telephone, a pager, an instant messaging device, a digital music player, a digital camera, or other devices that may be adapted to transmit and/or receive information

5 wirelessly. The system 500 may, for example, be used in any of the following systems: a wireless local area network (WLAN) system, a wireless personal area network (WPAN) system, or a cellular network, although the scope of the present invention is not limited in this respect.

10 The system 500 may include a controller 510, an input/output (I/O) device 520 (e.g., a keypad display), a memory 530, and a wireless interface 540 coupled to each other via a bus 550. It should be noted that the scope of the present invention is not limited to embodiments having 15 any or all of these components.

The controller 510 may comprises, for example, one or more microprocessors, digital signal processors, microcontrollers, or the like. The memory 530 may be used to store messages transmitted to or by the system. The 20 memory 530 may also be optionally used to store instructions that are executed by the controller 510. During the operation of the system 500 it may be used to store user data. The memory 530 may be provided by one or more different types of memory. For example, a memory 530 25 may comprise a volatile memory (any type of random access

memory), a non-volatile memory such as a flash memory, and/or phase change memory cells 10.

The I/O device 520 may be utilized to generate a message. The system 500 may use the wireless interface 540 5 to transmit and receive messages to and from a wireless communication network with a wireless radio frequency (RF) signal. Examples of the wireless interface 540 may include an antenna or a wireless transceiver, such as a dipole antenna, although the scope of the present invention is not 10 limited in this respect.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended 15 claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: